

AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0027] with the following context:

5 “[0027] It is appreciated to refer to Figs. 4-6 to realize the NVM cell structure. Fig. 4
is a cross-sectional diagram of the NVM cell shown in Fig. 3 along a line
A-A’, Fig. 5 is a cross-sectional diagram of the NVM cell shown in Fig. 3
along a line B-B’, and Fig. 6 is a cross-sectional diagram of the NVM cell
shown in Fig. 3 along a line C-C’. As shown in Fig. 4, the portion of the
10 NVM cell in the first region I includes a P-well 60 positioned in the
substrate 50, an isolation structure 62 positioned on the P-well 60, and a
stacked structure, which is composed of the control gate 52, an insulating
layer 64, and the floating gate 54, positioned atop the isolation structure 62.
In a better embodiment of the present invention, the substrate 50 is a P-type
15 silicon substrate, the insulating layer 64 is an ONO (oxide/nitride/oxide)
composite layer, the floating gate ~~[[52]]~~ 54 and the control gate ~~[[54]]~~ 52 are
formed of doped polysilicon or other conductive materials, and the isolation
structure 62 is either a field oxide layer or a shallow trench isolation
structure. Alternatively, the substrate 50, the P-well 60 and the N-type
20 doping region 58 can be formed into different conductive types, depending
on the circuit design to the NVM cell. Optionally, a deep N-well is formed
to provide a guard ring surrounding the NVM cell. In addition, the
insulating layer 64 can be formed of any materials endurable to high-voltage
operations.”

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